VERILOG DESIGN OF INPUT/OUTPUT PROCESSOR WITH BUILT-IN-SELF-TEST

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Specially dedicated to my beloved parents, younger brother, supervisor, lectures, fellow friends and those who have guided and inspired me throughout my journey of education.

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ABSTRACT

This project has a final goal of designing an I/O processor (IOP) with embedded built-in-self-test (BIST) capability. The IOP core design was originally design in VHDL modeling has been migrated to Verilog HDL modeling in this project. BIST is one of the most popular test technique used nowadays. The embedded BIST capability in IOP designed in this project has the objectives to satisfy specified testability requirements and to generate the lowest-cost with the highest performance implementation. Linear Feedback Shift Register (LFSR) is used to replace the expensive testers to generate pseudo random test pattern to IOP while Multiple Input Signature Register (MISR) is able to compact the IOP output response into a manageable signature size. In this project, the designed is coded in Verilog hardware description language at register transfer level (RTL), synthesized using Altera Quartus II using FPFA device from APEC20KE family, RTL level compilation and simulation using Modelsim v6.1b and gate level timing simulation using Modelsim-Altera v6.1g. This project was scheduled for two semester in which the activities to study and determine hardware specifications, requirements, functionalities and Verilog HDL migration were done in first semester whereas activities to design, synthesis, compile, simulate, and validate were carried out in semester 2. IOP with BIST capability contributes additional 30% hardware overhead but is somehow reasonable considering the test performance obtained and the ability of the BIST block provides high fault coverage.

ABSTRAK

Projek ini bertujuan untuk merekacipta satu pemproses masukan/keluaran (IOP) dengan keupayaan terbina dalam uji sendiri (BIST). Pada asalnya, IOP dimodel dalam bahasa VHDL telah ditukar kepada rekacipta dalam bahasa Verilog HDL. BIST merupakan salah satu teknik yang paling banyak diguna hari ini. Keupayaan BIST yang dimasukan ke dalam IOP bertujuan untuk memenuhi keperluan keujianan tertentu dan menjana kos yang paling rendah dengan prestasi yang paling tinggi. Pendaftar Anjakan Suap Balik Linear (LFSR) diguna untuk mengantikan penguji yang mahal and untuk menjana ujian yang pseudo rawak kepada IOP. Padahal, Pendaftar Tandatangan Pelbagai Masukan (MISR) boleh diguna untuk mengurangkan keluaran sambutan dalam untuk tandatangan yang boleh gurus. Dalam projek ini, IOP dimodel dalam bahasa Verilog dalam tahap pendaftar pindah (RTL), sistesis dengan menggunakan Altera Quartus II dengan FPGA dari keluarga APEC20KE, kompil rekacipta dalam tahap RTL, simulasi rekacipta dengan menggunakan Modelsim v6.1b dan simulasi tahap get dengan Modelsim-Altera v6.1g. Project ini dirancang bagi 2 semester dengan aktiviti untuk menentukan specifikasi rekacipta, keperluan dan fungsi rekacipta and ketukaran kepada IOP dalam bahasa Verilog dilaksanakan semasa semester 1, manakala aktiviti rekacipta, sistesis, kompil dan simulasi dilaksanakan dalam semester 2. IOP dengan keupayaan BIST terbina dalam menbesarkan IOP sebanyak 30%, tetapi dianggap boleh tahan and boleh diterima memandangkan prestasi uji yang cemerlang and keupayaan BIST untuk memberi liputan kesalahan yang begitu tinggi.

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LIST OF ABBREVIATIONS

ASIC	-	Applications Specific Integrated Circuit
ATPG	-	Automatic Test-Pattern Generation
BILBO	-	Built-In Logic Block Observers
BIST	-	Built-In-Self-Test
CAD	-	Computer Aided Design
CU	-	Control Unit
CUT	-	Circuit Under Test
DPU	-	Data Path Unit
DUT	-	Design Under Test
FES	-	Front End Subsystem
FPGA	-	Field Programmable Gate Array
HDL	-	Hardware Description Language
IC	-	Integrated Circuit
IP	-	intellectual property
LFSR	-	Linear Feedback Shift Register
LSB	-	Least Significant Bit
MISR	-	Multiple Input Signature Register
I/O	-	Input/Output
PC	-	Personal Computer
ROM	-	Read-Only-Memory
RTL	-	Register Transfer Level
UART	-	Universal Asynchronous Receiver/Transmitter
SDF	-	Standard Delay Format
XOR	-	Exclusive OR

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CHAPTER 1

INTRODUCTION

This chapter gives an overview of the whole project, starts with the project background and problem statement, followed by the project objectives, scopes, project contributions and thesis outline

1.1 Overview and Problem Statement

The UTM PC-based FPGA Prototyping System consists of the I/O Processor (IOP) core and the Front-End Subsystem. Please refer to thesis titled "*PC-Based FPGA Prototyping System – Front-End Subsystem Design" (2005)* by Ng, Shuh Jiuan and "*PC-Based FPGA Prototyping System – I/O Processor Design" (2005)* by Chua, Lee Ping for more detail of the system design. The system is designed to enable users to send input data to Design-Under-Test (DUT) and obtains the DUT outputs displays on the Personnel Computer (PC) screen. This project will focus on discussing the IOP with embedded Built-In-Self-Test capability design.

IOP is a soft core that can be used to handle data communication between the PC and DUT in the FPGA-based Prototyping Board. The UART module in IOP is a soft core that used to conduct serial I/O communication. A universal asynchronous receiver/transmitter (UART) is a type of asynchronous receiver/transmitter computer hardware which is used to translate data between parallel and serial interfaces. It is commonly used for serial data telecommunication. A UART converts bytes of data to and from asynchronous start-stop bit streams represented as binary electrical impulses. It is mainly used at broadband modem, base station, cell phone, and PDA designs

It is crucial that the IOP is functioning correctly and is fault free in real silicon or FPGA board to ensure that the data sends to the DUT inputs are correct and outputs from the DUT send back to the Front End Subsystem is reliable.

With the increasing growth of sub-micron technology has resulted in the difficulty of testing. Manufacturing processes are extremely complex, making the manufacturers to consider testability as a requirement to assure the reliability and the functionality of each of their designed circuits. Built-In-Self-Test (BIST) is one of the most popular test technique used. For design and test development, BIST significantly reduces the costs of automatic test-pattern generation (ATPG) and also reduces the likelihood of disastrous product introduction delays because of a fully designed system cannot be tested.

A Universal Asynchronous Receive/Transmit with BIST capability has the objectives of firstly to satisfy specified testability requirements, and secondly to generate the lowest-cost with the highest performance implementation. Although BIST slightly increases the cost because of the BIST hardware overhead in the design and test development, due to added time required to design and added pattern generators, response compactors, and testability hardware. However, it is normally less costly than test development with ATPG.

With the reasons discussed above, this project focuses on the design of the embedded BIST architecture for an IOP. The designs will be implemented using Verilog Hardware Description Language (HDL) at the Register Transfer Level (RTL) abstraction level. BIST technique will be incorporated into the IOP design before the overall design is synthesized by means of reconfiguring the existing design to match testability requirements.

1.2 Objectives

The main objective of this project is to design a serial I/O Processor (IOP) logic core with the Built-in-Self-Test (BIST) capability using Verilog HDL.

This entails the following sub-objectives:

1. To migrate the UTM serial I/O processor (IOP) from VHDL to Verilog HDL modeling.
2. To upgrade the I/O Processor with Built-In-Self-Test capability.
3. To explore the possibility for implementation of the I/O module design with Altera APEX20 family Field Programmable Gate Array (FPGA).

1.3 Scopes of Work

(a) IOP was originally design in using VHDL. It is converted to Verilog HDL design.

(b) IOP is upgraded with embedded BIST capability.

(c) The design is modeled in Verilog HDL at the RTL abstraction level.

(d) This project is limit to design, simulate, validate and verify the design at RTL level using Mentor Graphic's Modelsim v6.1 b.

(e) In this project, the design is synthesized into gate level netlist with Altera EP20K200EFC484-2X FPGA board using Altera's Quartus II 6.1.

(f) Gate level timing simulation, validation and verification will be performed using Modelsim-Altera 6.1g.

(g) The design is targeting based on opportunistic to implement into Altera's EP20K200EFC484-2X FPGA board.

1.4 Project Contributions

The IOP is migrated to Verilog HDL which contributes several advantages. Verilog HDL allows different levels of abstraction to be mixed in the same models and thus can define a hardware model in terms of switches, gates, RTL, or behavioral code. Besides, most popular logic synthesis tools support Verilog HDL. This makes it the language of choice for many ASIC companies. More important, all fabrication vendors provide Verilog HDL libraries for post logic synthesis simulation. Thus, designing a chip in Verilog HDL allows the widest choice of vendors. On top of that, compared to VHDL, Verilog HDL provides better code efficiency and easier to learn. Nowadays, most IC design company like Intel, Altera, Avago and other companies have migrated HDL design from VHDL to Verilog.

BIST is getting more and more important today. New ASIC (Applications Specific Integrated Circuit) designs nowadays are having embedded BIST. An IOP with BIST capability helps UTM Faculty of Electrical (FKE) in future research of the area of IC testing. This project also serves as a starting point and proof of concept. It can be a soft core IP (intellectual property) for UTM FKE and helps FKE to own its own IC design with BIST.

With the implementation of BIST, it enables to test IOP automatically through the self-generated test with exhaustive data values. This ensures the IOP chip is fault free by having very high fault coverage testing. With embedded BIST, expensive tester requirements and testing procedures starting from circuit or logic level to field level testing are minimized and this reduces the chip or system test cost. The reduction of the test cost will lead to the reduction of overall production cost.

IOP with BIST capability at the same time ensures the fault free circuit and thus making sure that the input data from Front End Subsystem through the IOP to DUT are correct as well as the DUT outputs values are reliable.

1.5 Thesis Outline

This thesis concentrates on the theory and design of IOP with embedded BIST capability and its functionality. This thesis is organized into 7 chapters. Chapter 1 is an overview of the project, objectives, project scope, project contributions and thesis outline. Chapter 2 discusses the project background, literature survey and theory which includes theory of serial communication, the UART and the overview of Built-In-Self-Test such as the BIST process, implementation, architecture and design

Chapter 3 elaborates the project methodology and the CAD design tools. It discusses the project design and implementation flow and CAD tools used in working out this project. Chapter 4 is the gives an overview 0f the UTM IOP design. This chapter includes the architecture of the IOP, messages format and IOP operations.

Chapter 5 describes core chapter of this thesis, which will describe in more detail the BIST module design includes the BIST architecture, operations, control unit as well as data path unit (DPU). Chapter 6 elaborates the simulation, results and analysis of IOP with embedded BIST capability. Finally, Chapter 7 concludes this project with conclusion, project limitations, recommendations and suggested future works.

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